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11 3 DFT1 - Test Mode

Operation (SSF \u0026 Delay

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Bushnell, Michael L., and Vishwani D. Agrawal.

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Essentials of Electronic Testing for Digital, Memory, and Mixed-signal VLSI Circuits. New York, NY: Springer, 2000. Syllabus This course examines the theory and practice of fault analysis, test generation, and design for testability for digital circuits and systems.

~~EECS 579 | Electrical & Computer Engineering at Michigan~~

FRONTIERS IN ELECTRONIC TESTING Consulting Editor Vishwani D. Agrawal Books in the series: Analog and Mixed-Signal Boundary-Scan: A Guide to the IEEE 1149.4 Test Standard A. Osseiran

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different test and design for testability methods.

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Instructor: Professor Vishwani D. Agrawal, vagrawal@eng.auburn.edu, Broun 323, 334-844-1853.

Text book: Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by Bushnell and Agrawal, Springer, 2000. HOMEWORK (30%): Homework 1 -- Problems 1.2 and 1.4, assigned 1/12/06, due 1/26/06, solution

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Copyright 2002 Publisher  
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978-0-306-47040-0 DOI  
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Scan 4 Scan Design Scan  
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using pre-specified design  
rules. Test structure  
(hardware) is added to the  
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control (TC) primary input.



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